CLAIMS:

1. A time-multiplexed data bus driver circuit for use in an emulation or prototyping system, the bus driver circuit comprising:

a plurality of combinatorial circuits, each of said circuits forming a logic combination of a datum value, a datum enable signal and a datum timeslot signal, said plurality of circuits producing a plurality of output signals based thereon, and

a wired-OR junction producing a logic OR combination of said plurality of output signals representing a time-multiplexed data stream.

2. The circuit of claim 1 which further comprises:

an emulator of a target system datum enable logic, wherein the circuit produces the same emulation result in the output signals that the target system datum enable logic would produce.

3. The circuit of claim 1, wherein for each of the combinatorial circuits the enable signal and the timeslot signal are combined in an AND function to produce a gating signal for the datum value, one selected datum value being gated onto the wired-OR junction at a given timeslot when enabled.

4. The circuit of claim 1, wherein the wired-OR junction includes a pre-charging circuit for actively driving said junction to a positive voltage.

5. The circuit of claim 1, wherein the wired-OR junction includes a pre-charging circuit for actively driving said junction to a ground voltage.

6. The circuit of claim 1, wherein a plurality of said timeslot enable signals input to a plurality of combinatorial circuits are connected in common.

7. The circuit of claim 1 which further comprises:

arbitration logic coupled with said plurality of combinatorial circuits for selectively enabling only one at a time the plurality of datum enable signals in such manner that only the selected one of the plurality of combinatorial circuits drives the time-multiplexed data bus in any given time slot, said arbitration logic causing each of the non-enabled ones of the plurality of combinatorial circuits to drive its output signal into a defined high-impedance state.

8. The circuit of claim 7, wherein said arbitration logic is synchronized with a system clock signal to assert the selected one of the plural datum enable signals a defined period of time prior to the arrival of the datum timeslot signal.

9. The circuit of claim 8 which further comprises:

timeslot generation logic coupled with said plurality of combinatorial circuits for producing the plurality of datum timeslot signals.

10. The circuit of claim 9 wherein a plurality of said datum timeslot signals input to a plurality of combinatorial circuits are connected in common.

11. The circuit of claim 10 wherein for each of the combinatorial circuits the enable signal, the timeslot signal and the datum signal are combined in an AND function to produce a gating signal for an active-low datum value, one selected active-low datum value being gated onto the wired-OR junction at a given timeslot when enabled.

12. The circuit of claim 11 wherein the wired-OR junction includes a pre-charge circuit for actively driving said junction to a positive voltage.

13. The circuit of claim 11 wherein the wired-OR junction includes a pre-charge circuit for actively driving said junction to a ground voltage.

14. A time-multiplexed system comprising:

a plurality of combinatorial circuits, each of said circuits forming a logic combination of a datum value, a datum enable signal and a datum timeslot signal, said plurality of circuits producing a plurality of output signals based thereon;

arbitration logic coupled with said plurality of combinatorial circuits for selectively enabling only one at a time the plurality of datum enable signals in such manner that only the selected one of the plurality of combinatorial circuits drives the time-multiplexed data bus in any given time slot, said arbitration logic causing each of the non-enabled ones of the plurality of combinatorial circuits to drive its output signal into a defined high-impedance state;

timeslot generation logic coupled with said plurality of combinatorial circuits for producing the plurality of datum timeslot signals; and

a wired-OR junction producing a logic OR combination of said plurality of output signals representing a time-multiplexed data stream, said wired-OR junction being biased to a positive voltage,

wherein for each of the combinatorial circuits the enable signal, the timeslot signal and the datum signal are combined in an AND function to produce a gating signal for an active-high datum value, one selected active-high datum value being gated onto the wired-OR junction at a given timeslot when enabled such that said wired-OR junction forms a common time-multiplexed data channel representing in an un-driven state a logic 0.

15. The system of claim 14, wherein a plurality of said datum timeslot signals input to a plurality of combinatorial circuits are connected in common.

16. The system of claim 15, wherein said arbitration logic is synchronized with a system clock to assert the selected one of the plural datum enable signals a defined period of time prior to the arrival of the datum timeslot signal.

17. The system of claim 14 which forms a part of an emulation system wherein said combinatorial circuits, said arbitration logic and said timeslot generation logic are part of a system being emulated and the time-multiplexed data channel is part of an emulator.

18. The system of claim 14 wherein said junction is biased to a positive voltage by a pre-charge circuit including a transistor that actively drives said junction to the positive voltage.

19. The system of claim 14 wherein said junction is biased to a positive voltage by a pull-up resistor.

20. A time-multiplexed system comprising:

a plurality of combinatorial circuits, each of said circuits forming a logic combination of a datum value, a datum enable signal and a datum timeslot signal, said plurality of circuits producing a plurality of output signals based thereon;

arbitration logic coupled with said plurality of combinatorial circuits for selectively enabling only one at a time the plurality of datum enable signals in such manner that only the selected one of the plurality of combinatorial circuits drives the time-multiplexed data bus in any given time slot, said arbitration logic causing each of the non-enabled ones of the plurality of combinatorial circuits to drive its output signal into a defined high-impedance state;

timeslot generation logic coupled with said plurality of combinatorial circuits for producing the plurality of datum timeslot signals; and

a wired-AND junction producing a logic AND combination of said plurality of output signals representing a time-multiplexed data stream, said wired-AND junction being biased to a ground voltage,

wherein for each of the combinatorial circuits the enable signal, the timeslot signal and the datum signal are combined in an AND function to produce a gating signal for an active-low datum value, one selected active-low datum value being gated onto the wired-OR junction at a given timeslot when enabled such that said wired-AND junction forms a common time-multiplexed data channel representing in an un-driven state a logic 1.

21. The system of claim 20, wherein a plurality of said datum timeslot signals input to a plurality of combinatorial circuits are connected in common.

22. The system of claim 21, wherein said arbitration logic is synchronized with a system clock to assert the selected one of the plural datum enable signals a defined period of time prior to the arrival of the datum timeslot signal.

23. The system of claim 18 which forms a part of an emulation system wherein said combinatorial circuits, said arbitration logic and said timeslot generation logic are part of a system being emulated and the time-multiplexed data channel is part of an emulator.

24. The system of claim 18 wherein said junction is biased to a ground voltage by a pre-charge circuit including a transistor that actively drives said junction to the ground voltage.

25. The system of claim 18 wherein said junction is biased to a ground voltage by a pull-down resistor.